ABSTRACT

Systems and methods of predicting instruction branches provide for independent checking predictions and dynamic next-line predictions. Next-line predictions may also have a latency that is a plurality of clock cycles, where the next line predictions include group predictions. Each group prediction includes a plurality of target addresses corresponding to their plurality of clock cycles. The plurality of target addresses can include a leaf target and one or more intermediate targets, where the leaf target defines a target address of the group prediction.

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